REMARKS/ARGUMENTS

1. Rejection of claims 1-5, 7-12, 14 and 15 as being anticipated by Schadt et al. (US Patent 6,870,395):

Claim 1:

Claim 1 A method for implementing circuit layouts in a chip, comprising:

forming a plurality of sub-circuit cells with the same layout in different positions of the chip; and

when the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connection layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells.

The Examiner has asserted that Schadt teaches the method for implementing circuit layouts in a chip of the claimed invention. The applicant respectfully disagrees.

First, the Examiner indicates that Schadt teaches forming a plurality of sub-circuit cells with the same layout in different positions of the chip. In fact, Schadt only teaches that the PLD 200 includes a number of standard-cell logic blocks (SLB) 220 located around the periphery of the device in regions that were underutilized in FPGA 100 (see col. 3 lines 40-42, and Fig. 2), and each SLB 220 includes the same type of standard-cell logic (see col. 4, lines 3-6). Therefore, Schadt only teaches that the SLBs 220 include the same type of logic devices, but *he **never** teaches that the SLBs 220 have **the same layout** in different positions*. Each SLB 220 having the same type of standard-cell logic does not signify that the SLBs 220 located in different positions have the same layout. The number

and arrangement of standard-cell logic of the SLBs 220 may be different in different positions according to Schadt's teaching.

In addition, the Examiner says that Schadt teaches when the sub-circuit cells in different positions require different circuit functions, performing a layout programming in at least a connection layer so that different layouts are formed in different positions of the connection layer corresponding to the sub-circuit cells as claim 1 claims. However, Schadt teaches uses software control to provide different functions, rather than forming different layouts in different positions of the connection layer. The applicant explains the difference as follows:

Schadt discloses two connectivity structures including perimeter-based connectivity structure for programmably connecting each SLB to either I/O buffers, programmable logic core, or both, and core-based connectivity structure for programmably connecting each SLB to either memory blocks, programmable logic core, or both. However, the programmability of the connectivity structures is achieved in a software control manner. Please refer to col. 4, line 57 to col. 5, line 26, and Fig. 3, the programmable connectivity of Schadt's teaching is provided by the **switch box 302** via routing resources 304 between SLB 220, logic blocks 206, and muxes/demuxes 212 corresponding to I/O buffers 210. Switch box 302 and routing resources 304 form part of the first, perimeter-based connectivity structure of PLD 200. Similarly, switch box 306 (e.g. another set of muxes) provides programmable connectivity via routing resources 308 between SLB 220, logic blocks 206, and memory blocks 208. Switch box 306 and routing resources 308 form part of the second, core-based connectivity structure of PLD 200. The muxes in switch boxes 302 and 306 are independently programmable to provide flexible connectivity between the various elements of PLD 200. In particularly, switch boxes 302 and 306 can be **programmed via software control** to provide signal flow in a variety of ways between SLB 220 and the rest of PLD 200.

On the other hand, the present application teaches performing a **layout programming** in at least a connection layer so that different layouts are formed in different positions **of the connection layer** corresponding to the sub-circuit cells when the sub-circuit cells in different positions require different circuit functions. It is the connection layer that has different layouts in different positions corresponding to the cub-circuit cells, and it is the connection layer that provides the programmability. The required function is selected when the connection layer is formed, rather than after the connection layer is formed.

In summary, the programming of the present application is achieved **when the connection layer is formed**, but the programming of Schadt's teaching is carried out by **controlling the switch boxes in a software manner after the PLD is completed**. Therefore, claim 1 is distinct from Schadt's teaching, and should be allowed. Reconsideration of claim 1 is politely requested.

Claims 2, 5, 7-8:

Claims 2, 5, and 7-8 are dependent on claim 1, and should be allowed if claim 1 is found allowable. Reconsideration of claims 2, 5, and 7-8 are politely requested.

Claim 3:

Claim 3 teaches that the layout programming is only performed in the connection layer so that the sub-circuit cells with different circuit functions have different layouts only in the connection layer. Schadt's connection layer surely has the same layout when different functionality is required, because the programming is done by the switch boxes in a software control manner after the connection layer is formed. Thus, claim 3 should be

allowed, and reconsideration of claim 3 is politely requested.

Claim 4:

Claim 4 teaches that while performing the layout programming, **each layout in the connection layer** corresponding to each sub-circuit cell is **selectively connected** to the sub-circuit blocks of each sub-circuit cell so that the sub-circuit cells in different positions implement different circuit functions. The programming is achieved by the switch boxes in a software control manner after the connection layer is formed, and therefore Schadt's connection layer cannot be selectively connected to the SLB and other components. Thus, claim 4 should be allowed, and reconsideration of claim 4 is politely requested.

Claim 9:

Claim 9 A chip, comprising:

a plurality of layout layers comprising a plurality of same layouts in a plurality of positions of the layout layers so as to implement a plurality of sub-circuit cells with the same layout; and

at least a connection layer comprising different layouts corresponding to the different positions of the layout layers so that the sub-circuit cells in different positions implement different circuit functions.

The Examiner has asserted that Schadt teaches the chip of the claimed invention. The applicant respectfully disagrees.

First, the Examiner indicates that Schadt teaches the chip comprising a plurality of layout layers comprising a plurality of same layouts in a plurality of positions of the layout layers so as to implement a plurality of sub-circuit cells with the same layout as

claim 9 claims. However, Schadt only teaches that the PLD 200 includes a number of standard-cell logic blocks (SLB) 220 located around the periphery of the device in regions that were underutilized in FPGA 100 (see col. 3 lines 40-42, and Fig. 2), and each SLB 220 includes the same type of standard-cell logic (see col. 4, lines 3-6). Therefore, Schadt only teaches that the SLBs 220 includes the same type of logic devices, but *he* ***never*** *teaches that the SLBs 220 have* ***the same layout*** *in different positions*. Each SLB 220 having the same type of standard-cell logic does not signify that the SLBs 220 located in different positions have the same layout. The standard-cell logic may be arranged in different SLBs 220 in different positions according to Schadt's teaching.

In addition, the chip of the present application comprises at least a connection layer comprising different layouts corresponding to the different positions of the layout layers so that the sub-circuit cells in different positions implement different circuit functions. On the other hand, Schadt's teaches that depending on the available area and the functionality to be supported, one or more **different SLBs** may be implemented within each region 216 or 218 in PLD 220. This only signifies that different functionalities are supported by different SLBs. The programmable connection is, however, achieved by the switch boxes, instead of different layouts of the connection layer. Thus, claim 9 is distinct from Schadt's teaching, and claim 9 should be allowed. Reconsideration of claim 9 is politely requested.

Claims 10, 12, 14-15:

Claims 10, 12, and 14-15 are dependent on claim 9, and should be allowed if claim 9 is found allowable. Reconsideration of claims 10, 12, and 14-15 are politely requested.

Claim 11:

Claim 11 teaches that each sub-circuit cell comprises a plurality of sub-circuit blocks, and the layouts of the connection layer are selectively connected the sub-circuit blocks of each sub-circuit cell so that the sub-circuit cells in different positions implement different circuit functions. The programming is achieved by the switch boxes in a software control manner after the connection layer is formed, and therefore Schadt's connection layer cannot be selectively connected to the SLB and other components. Thus, claim 11 should be allowed, and reconsideration of claim 11 is politely requested.

2. Allowable Subject Matter:

Claim 6:

Claim 6 should not be objected and should be allowed if claim 1 is found allowable.

Claim 13:

Claim 13 should not be objected and should be allowed if claim 9 is found allowable.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 10/13/2006

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)